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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/709,004	04/07/2004	Yuan-Kun Hsiao	320528626US2	3003		
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PERKINS COIE LLP			SINGH, HIRDEPAL			
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/709,004	HSIAO, YUAN-KUN	
	<b>Examiner</b>	<b>Art Unit</b>	
	HIRDEPAL SINGH	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 31 March 2008.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-31 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1,2,6-22 and 26-31 is/are rejected.  
 7) Claim(s) 3-5, 23-25 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
     1. Certified copies of the priority documents have been received.  
     2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
     3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>10/29/2007, 12/16/2007</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
|   | 6) <input type="checkbox"/> Other: _____ .                        |

## **DETAILED ACTION**

1. This action is in response to the amendment filed on March 31, 2008. Claims 1-31 are pending and have been considered below.

### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-31 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 6, 11-15, 18, 20-22, 26 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915) in view of Chou (US 2003/0048120).

#### **Regarding claims 1, 12, 15 and 21:**

Minamino et al discloses a clock generator being applied to a DVD optical drive (abstract; paragraphs 0002 and 0042) for generating a non-phase-modulated target clock signal based on a phase-modulated input signal, the clock generator comprising: a phase-locked loop (paragraph 0007) connected to the arithmetic/logic circuit for generating the target signal according to the first control signal (paragraph 0054-0055

and ), and the input signal, feeding the target signal back to the input of the phase-locked loop, and determining whether the target clock signal is to be synchronized with the input signal based on the logic level of the first control signal (paragraphs 0076-0077);

wherein when the first control signal corresponds to a first logic level (paragraph 0076), the phase-locked loop compares the target clock signal with the input signal to drive the target clock signal to be synchronized with the input signal, and when the first control signal corresponds to a second logic level (paragraph 0076), the phase-locked loop holds the target clock signal without driving the target clock signal to be synchronized with the input signal.

Minamino further discloses an arithmetic/logic circuit (307 in figures 3-4) for calculating a period count value by counting (413 in figure 4; paragraph 0050) a period of the input signal according to a reference clock, calculating an average value, and comparing the average value with the period count value for outputting a first control signal (output of 407 in figure 4; paragraph 0053), except for specifically teaching that the counter is calculating a period count value by counting a period of the input signal according to a reference clock and averaging a plurality of the period count values, and comparing the average value and period count value.

However, Chou in the same field of endeavor discloses a system and method for clock generation and recovery where a counter (72 in figure 7) is calculating a period count value by counting a period of the input signal according to a reference clock (paragraphs 0033-0034) and averaging a plurality of the period count values (74, 76 in

figure 7), and comparing the average period value and period count value (78 in figure 7; paragraphs 0037-0038).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use teachings of Chou in the Minamino system to count a period of input and compare the average and the count value itself in order to generate control signal based and stop the comparison as a predefined condition is met that helps in distinguishing between different frequencies of wobble signal for better clock generation and recovery in the optical disk systems.

**Regarding claims 2, 13 and 22:**

Minamino et al discloses all of the subject matter as described above and further discloses that the circuit comprises;

reference clock generator generating a reference clock having predetermined frequency (304 in figure 3; paragraph 0049);

a counter connected to reference clock generator counting the number of period according the input or wobble signal (306 in figure 3; paragraph 0050);

a mean or average unit for calculating the average of count number (406 in figure 4; paragraph 0054);

a controller which generates a control signal according to the average value and the rectification value is doing the same function as the comparator in the claimed invention (407 in figure 4; paragraph 0055).

**Regarding claims 6, 18 and 26:**

Minamino et al discloses all of the subject matter as described above and further discloses that when the phase difference between signal and encoded sub code frame synchronization signal is a predetermined value the reference clock is the write clock signal (paragraph 0016) except for specifically teaching that when difference between count value and the average value is less than a critical value first control signal is set to a first logic level.

However, it would have been obvious to one of ordinary skill in the art at the time of invention to use the count value and average value of the Minamino device and compare the difference with a predetermined value to decide the logic level of the control signal. One would have been motivated to use the count value and average value to decide the logic level of control signal so that the generated clock signal from the PLL is in the correct phase.

**Regarding claims 11, 20 and 31:**

Minamino et al discloses all of the subject matter as described above and further discloses that clock generating device may be applied to an optical disc drive as DVD (paragraphs 0002 and 0042), and also discloses that the optical disc recorder simultaneously generate the encoder frame synchronization signal corresponding to each ADIP (paragraph 0016), except for specifically teaching that a second control signal is generated to prohibit the PLL to synchronize the target clock with the input signal at a predetermined time.

However, it is inherent that the absolute timing of the input signal is used to prevent PLL to synchronize the target clock with the input signal at a predetermined

time. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to prohibit the PLL from synchronizing the target clock with the input. One would have been motivated not to synchronize the target clock with the input signal at a predetermined time to keep the signal from being unstable.

**Regarding claim 14:**

Minamino et al discloses all of the subject matter as described above and further discloses generating an average value based on the period count value (paragraph 0054) except for specifically teaching that when average value equals an initial value the comparison between average and count value stops.

However, it is inherent that the average value processor stops comparison with a predefined condition whether it is when the count value becomes equal to the average value.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to generate control signal based on the comparison and stop the comparison as a predefined condition is met. One would have been motivated to use the comparison of average and periods count values to generate the control signal and stop comparing when the period count value equals the average value.

5. Claims 7, 19 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915) in view of Chou (US 2003/0048120) as applied to claims 1, 12 and 21 above, and further in view of Jahene et al. (US 7,039,380).

**Regarding claims 7, 19 and 27:**

Minamino et al discloses all of the subject matter as described above except for specifically teaching that when difference between plurality of consecutive period count values and the average value are less than a critical value first control signal is set to a first logic level.

However, Jahene et al discloses that when the phase difference is less than a predetermined value the reference clock is the write clock signal (column 2, lines 30-45), and further discloses that the first reference synchronization signal is generated based on the average value of plurality of count values which in turn controls the PLL (figure 5; column 3, lines 56-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the difference between plurality of consecutive period count values and the average value of the Minamino device and compare the difference with a predetermined value to set the logic level of the control signal. One would have been motivated to set the logic level of control signal according to the difference between plurality of consecutive period count values and the average value to generate clock signal that is in the correct phase.

6. Claims 8-9, 16-17 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915) in view of Chou (US 2003/0048120) as applied to claims 1, 12 and 21 above, and further in view of Van Vlerken et al. (US 6,765,861).

**Regarding claims 8, 16 and 28:**

Minamino et al discloses all of the subject matter as described above except for specifically teaching that when difference between period count value and the average value is larger than a critical value first control signal is set to a second logic level.

However, Van Vlerken et al discloses that when the phase difference is less than a predetermined value the reference clock is the write clock signal (column 2, lines 1-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the count value and average value and compare the difference with a predetermined value and set the logic level of the control signal to a second logic level if the difference is large or smaller than the predetermined value. One would have been motivated to use the difference between period count value and average value to set the logic level of control signal to a second logic level if the difference is larger than a predetermined value so that the generated clock signal is in the correct phase and does not get altered during the phase modulated cycles of the wobble signal.

**Regarding claims 9, 17 and 29:**

Minamino et al discloses all of the subject matter as described above except for specifically teaching that when difference between plurality of consecutive period count values and the average value is larger than a critical value first control signal is set to a second logic level.

However, Van Vlerken et al discloses that when the phase difference is less than a predetermined value the reference clock is the write clock signal (column 2, lines 1-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the count value and average value and compare the difference with a predetermined value and set the logic level of the control signal to a second logic level if the difference is large than the predetermined value. One would have been motivated to use the difference between period count value and average value to set the logic level of control signal to a second logic level if the difference is larger than a predetermined value so that the generated clock signal is in the correct phase and does not get altered during the phase modulated cycles of the wobble signal.

7. Claims 10 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915) in view of Chou (US 2003/0048120) as applied to claims 1, 12 and 21 above, and further in view of Okamoto et al. (US 6,587,417).

**Regarding claims 10 and 30:**

Minamino et al discloses all of the subject matter as described above except for specifically teaching that the clock generating device has a band pass filter.

However, Okamoto discloses a similar method and device for clock generation and further discloses that the device includes a band pass filter and the output of the band pass filter is fed to the level slicer (abstract; figure 13; column 15, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the band pass filter and slicer to select the frequency and level of input signal. One would have been motivated to use the band pass filter and slicer at

the input of clock generator to get the controlled input signal with limited amplitude and frequency.

***Allowable Subject Matter***

8. Claims 3-5 and 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
9. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record Minamino et al discloses a system and method for generating and recovering a clock in optical disk drives where a count value is calculated by counting input signal period based on reference clock and a control signal is generated based on comparison of count and its average and further synchronizing the generated clock that is based on control signal and input signal in a predetermined way. But, prior art of record fails to discloses or teach that a second control signal is generated based on the comparison of input and the clock signal that was generated with first control signal i.e. the target clock and making a determination in accordance with the logic level of first control signal, and controlling frequency of target signal based on control voltage generated by loop filter according to second control signal.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Park et al. (US 2003/0099180) discloses a system and method for encoding and decoding a wobble signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HIRDEPAL SINGH whose telephone number is (571) 270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off) 8:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. S./  
Examiner, Art Unit 2611  
/Shuwang Liu/  
Supervisory Patent Examiner, Art Unit 2611